Single Barrier Varactors for Submillimeter Wave Power Generation

Svein M. Nilsen, Hans Grönqvist, Hans Hjelmgren, Anders Rydberg, and Erik L. Kollberg, *Fellow, IEEE*

***Abstract*—Theoretical work on Single Barrier Varactor (SBV) diodes indicates that the efficiency of a tripler with a SBV diode has a maximum for a considerably smaller capacitance variation than previously thought. SBV diodes based on GaAs, InGaAs and InAs have been fabricated, and their dc properties have been tested. Detailed modelling of the carrier transport properties of the SBV device is carried out in two steps. First, the semiconductor transport equations are solved simultaneously using a finite difference scheme in one dimension. Secondly, the calculated IV-, and CV characteristics are used by a multiplier simulator to calculate the optimum impedances, and output powers at the frequencies of interest. We have developed an analysis technique which complements the harmonic balance technique. Finally, simulations for a case study of a 750 GHz multiplier show that InAs diodes perform favorably compared to GaAs diodes.**

I. Introduction

A SINGLE BARRIER VARACTOR (SBV) device, consists of a thin layer of a large bandgap material that acts as a barrier, and a thicker layer of a smaller bandgap material on each side of the barrier [1]–[5], [7]. The cross section of a typical SBV diode is shown in Fig. 1. Since a symmetrical heterojunction structure has an antisymmetrical IV and a symmetrical CV characteristic around zero bias voltage, an applied RF voltage without any dc bias will only cause the generation of odd harmonics. This makes it possible to design higher order multipliers with fewer idler circuits and hence lower losses. The design procedure, and the mechanical construction of a higher order multiplier making use of a SBV device will thus become much easier compared to one which use a Schottky diode.

II. SBV Diodes

2.1 On the Design of SBV Devices

In designing SBV diodes, it is of considerable interest to have a good understanding of how the shape of the CV characteristic, and the series resistance R_s affect the multiplier performance. In this section we will briefly investigate the importance of R_s, the minimum capacitance $C_{\min}$ and the capacitance swing $(C_{\max} - C_{\min})$. The often quoted dynamic cutoff frequency, $f_{cd} = [1/(2\pi R_s C_{\min})] \times (1 - C_{\min}/C_{\max})$, [6], where R_s is the series resistance, suggests that $C_{\min}$ should be as small as possible, while $C_{\max}$ should be as large as possible. However, calculations show that, under the constraint that $C_{\min}$ is fixed, there exists an optimum $C_{\max}/C_{\min}$ ratio. It will also become evident that for most practical cases, i.e., when $C_{\max}/C_{\min} > 2$, $C_{\min}$ is much more important for the impedance level of the diode than is $C_{\max}$.

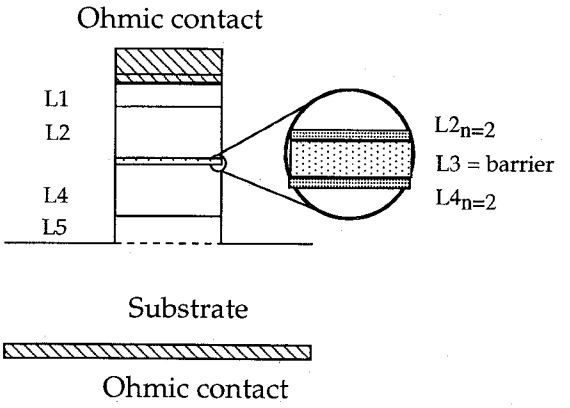

Fig. 1. Schematic cross section of a SBV mesa diode. $L1$ is the highly doped contact layer, $L2_n$ and $L4_n$ are the depletion regions on each side of the barrier (index n denotes sublayers), $L3_n$ is the barrier and $L5$ is part of the buffer/substrate layer. In the carrier transport simulator $L1$ and $L5$ are always equal. Mesa diameter = a.

For a particular simple case we choose to perform the analysis using the CV characteristic shown in Fig. 2 and to assume that all harmonics, except the first harmonic ω_p (pump frequency) and third harmonic $3\omega_p$ (output frequency) are short circuited over the variable capacitance. The dc bias voltage is always zero volts, and the maximum RF voltage over the diode is $|V(t)|_{\max} = V_{\max}$ (see Fig. 2). Checking this technique against a full harmonic balance technique reveals a very close agreement.

In Fig. 3 we have plotted the calculated efficiency η versus $C_{\max}/C_{\min}$ for different values of R_s, assuming $1/(\omega_p C_{\min}) = 100\,\Omega$ and that the diode is matched at the input and output ports. Fig. 4 shows optimum source $(R1, X1)$, and load $(R3, X3)$ impedances versus series resistance for the $C_{\max}/C_{\min}$ ratio yielding maximum efficiency, again with $1/(\omega_p C_{\min}) = 100\,\Omega$. We also find that $R1$, and $R3$ versus $C_{\max}/C_{\min}$ do not change much near the $C_{\max}/C_{\min}$ value yielding maximum efficiency. This is in accordance with the fact that the efficiency (proportional to $[(R1 - R_s)/R1] \times [(R3/(R3 + R_s)])$ does not vary much near its maximum (for $2 < C_{\max}/C_{\min} < 4$, see Fig. 3). Notice that in Fig. 4 we have

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S. M. Nilsen, H. Grönqvist, H. Hjelmgren, and E. L. Kollberg are with The Millimetre Wave Group, Department of Microwave Technology, Chalmers University of Technology, Rännvagen 6, S-412 96 Goteborg, Sweden.

A Rydberg is with the Circuits and Systems Group, Department of Technology, Uppsala University, Box 534, S-751 21 Uppsala, Sweden.

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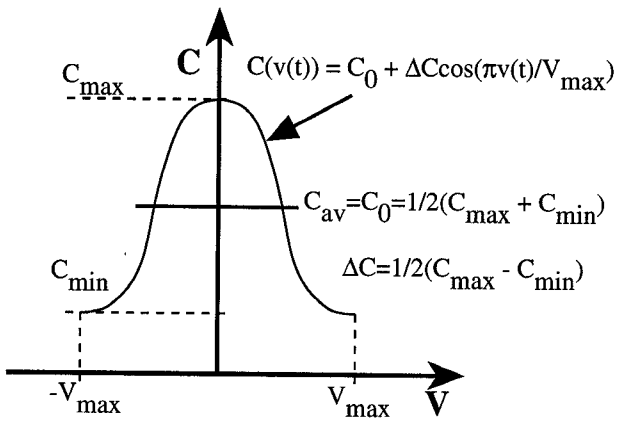

Fig. 2. CV characteristic of SBV diode used in the simplified analysis. $V_{\max}$ is the maximum voltage across the diode.

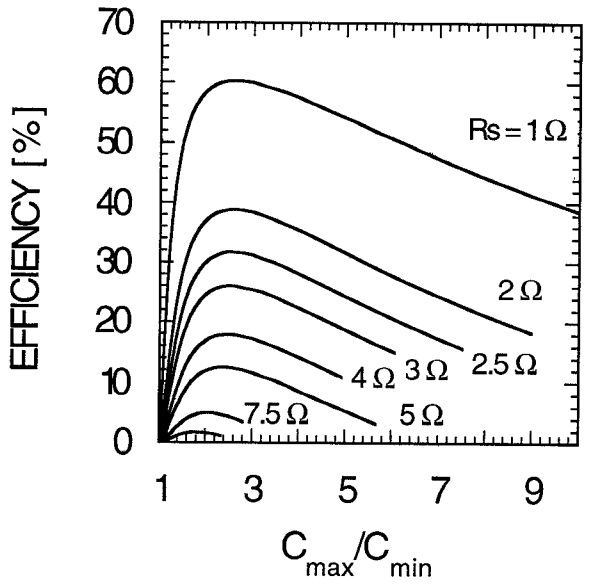

Fig. 3. Calculated efficiency versus $C_{\max}/C_{\min}$ ratio for series resistance (R_s) values of 1, 2, 2.5, 3, 4, 5, 7.5, and 10 Ω for a diode with a CV characteristic according to Fig. 2 and with $1/(\omega_p C_{\min}) = 100\,\Omega$.

not depicted the embedding impedance (Z_{emb}), but the proper input and output impedancies (at the input $Z_{\text{emb}} = Z_{\text{input}}$, at the output $Z_{\text{emb}} = Z_{\text{load}} + R_s$). The impedance values shown in Fig. 4 are normalized by our choice of $1/(\omega_p C_{\min}) = 100\,\Omega$, i.e., doubling $1/(\omega_p C_{\min})$ doubles all other impedance values as well. The results presented in Figs. 3 and 4 do not change much if the higher order embedding impedances are 377 Ω rather than short circuited.

A conclusion drawn from this simplified analysis is that for any given $\omega_p R_s C_{\min}$ there is a broad efficiency maximum for approximately $2 < C_{\max}/C_{\min} < 4$, see Fig. 3. The ratio should never be less than 2, while a too large $C_{\max}$ value will reduce the multiplier's efficiency. Furthermore, the source and load impedances for $C_{\max}/C_{\min} > 2$ were found to essentially be proportional to $1/(\omega_p C_{\min})$. These results can be used as rules of thumb in a diode design procedure, which in practice is rather elaborate, since parameters such as available input power, diode area, doping profiles, avalanche breakdown, current saturation, and maximum barrier thickness

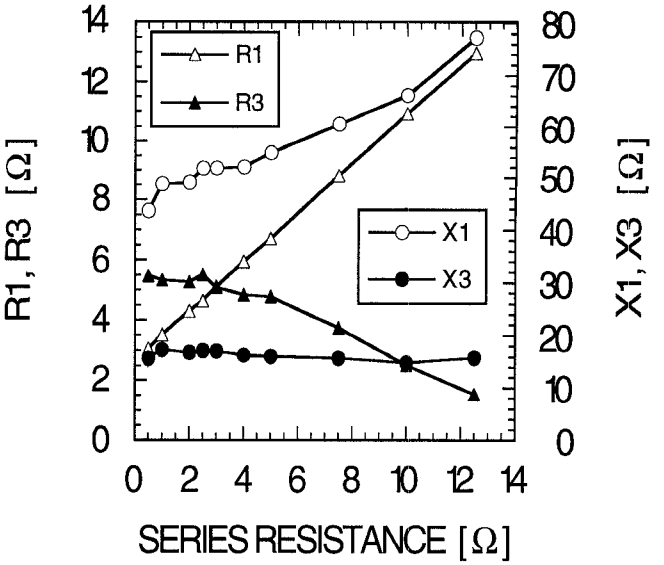

Fig. 4. Calculated source ($R1, X1$) impedance, and load ($R3, X3$) impedance (different from embedding impedance) versus series resistance for a tripler at maximum efficiency with $1/(\omega_p C_{\min}) = 100\,\Omega$.

(a too thick barrier will for some materials deteriorate the quality of the epilayer lattice) must be considered. We will discuss the design of SBV mateial in Section 2.4 below.

2.2 DC Measurements

The first experiments with a SBV multiplier [2] used diodes fabricated in GaAs with $Al_{0.7}Ga_{0.3}As$ barriers. It was found that this type of barrier was quite leaky due to indirect transitions [7], see Fig. 5. Improved performance is expected for a barrier composed of $Al_{0.44}Ga_{0.56}As$. It is indeed important to keep the conduction current through the diode low (di/dv small compared to $1/\omega C$)), since it will otherwise deteriorate the multiplier performance (see Section III and Fig. 12). Further improvement is expected from GaInAs materials. We have fabricated several diodes based on the materials GaAs, $In_{0.53}Ga_{0.47}As$ and InAs (see Table I for details). In the $In_{0.53}Ga_{0.47}As$ based diode a barrier of $In_{0.52}Al_{0.48}As$ was used. The latter diode was grown lattice matched to an InP substrate. For the InAs diodes we used an AlSb barrier that gives a high barrier, 1.3 eV for indirect transitions and ≈2 eV for direct [8]. It is therefore very efficient in blocking the current through the varactor. The influence of the epilayer design on the IV-, and CV characteristics has been investigated theoretically in Section 2.3.

The different SBV diodes fabricated by us have been dc characterized using a Hewlett Packard 4145B parameter analyzer. Most of the measurements have been done on large area diodes, 100–2500 μm^2. A limited number of measurements have been made on small area ($7\,\mu m^2$) diodes of the GaAs type (ID #614). DC characterization of the different SBV diodes shows that the current density decreases as expected when the barrier height increases, see Fig. 5. The lowest current density is obtained for InAs/AlSb devices as expected. Unfortunately, these devices also show

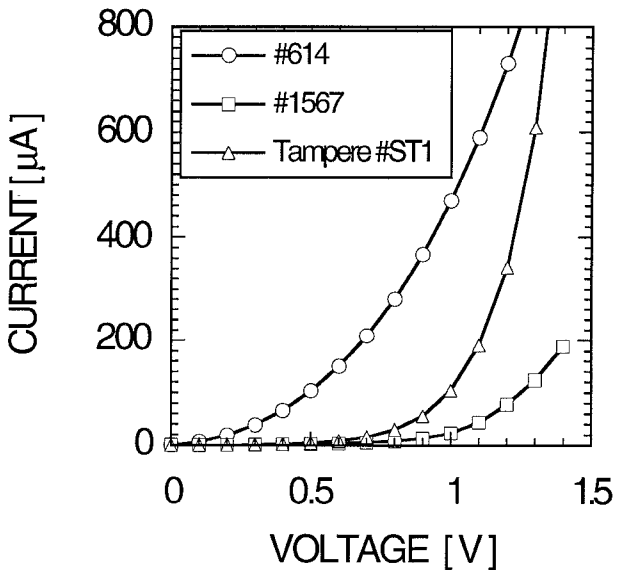

Fig. 5. Measured current versus voltage for SBV diodes of size $25 \times 25\ \mu m^2$ in different material systems. See Table I for details. A current of 800 μA corresponds to a current density of 128 A/cm^2.

a large variation (a factor of two or more) in current density. Whether this variation is caused by defects, due to the lattice mismatch or by some growth parameter, is not clear at the present. In comparison, diodes made from the lattice matched $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ material grown on an InP substrate, as well as those made from $GaAs/Al_{0.7}Ga_{0.3}As$ show current density variations of only a few per cent over the same distance. The measured breakdown voltages (voltage at which the device is destroyed) are low for the InAs and InGaAs diodes, about 2 V, in comparison with 6 V for the GaAs diode. These results are in agreement with the theory for avalanche breakdown [15], except for $In_{0.53}Ga_{0.47}As$. The breakdown voltage can be increased by using a lower doping concentration in the depletion regions. Notice however, that a lower doping concentration will increase the series resistance, and will decrease the maximum possible conduction current through the diode, causing possible current saturation problems [4]. A more efficient method for allowing a larger voltage swing is to use several barriers [4] and corresponding depletion regions in series. Each of the n identical "diodes" will then only need to sustain the total pump voltage divided by n. The n-fold increase in impedance can be compensated for by a corresponding n-fold increase in diode area. This approach will decrease the series resistance, partly because the spreading resistance of a larger area diode is lower, and partly because the mesa contribution is proportional to the number of depletion/electron drift regions, $n+1$. The power handling capacity increases with a factor of n^2.

2.3 Theoretical CV and IV Modelling of SBV Devices

To calculate the CV-, and IV characteristics, the semiconductor transport equations are solved simultaneously using a finite-difference scheme. The computer program is a modified version of a program for $GaAs/Al_xGa_{1-x}As/GaAs$ heterojunction structures developed by Hjelmgren [9], [10].

TABLE I
MATERIALS FROM WHICH SBV DIODES OF VARIOUS SIZES HAVE BEEN FABRICATED

Wafer ID, Supplier	Material system	Layer thicknesses (top/down) and doping concentration
# 614 IMEC	GaAs/$Al_{0.7}Ga_{0.3}As$/GaAs Buffer: n+ GaAs Substrate: n+ GaAs Barrier thickness L3	L1 = 400 nm, $N_d = 3.4\times10^{18}$ cm^{-3} $L2_1$ = 533 nm, $N_d = 1.0\times10^{17}$ cm^{-3} $L2_2$ = 5.3 nm, undoped L3 = 21.3 nm, undoped $L4_2 = L2_2$, $L4_1 = L2_1$ L5 = 1998 nm, $N_d = 3.4\times10^{18}$ cm^{-3}
# 1566 Chalmers	InAs/AlSb/InAs Buffer: n+ InAs, and n+ GaAs Substrate: n+ GaAs Barrier thickness L3	L1 = 200 nm, $N_d = 5.0\times10^{18}$ cm^{-3} $L2_1$ = 400 nm, $N_d = 6.0\times10^{16}$ cm^{-3} $L2_2$= 5 nm, undoped L3 = 20 nm, undoped $L4_2 = L2_2$, $L4_1 = L2_1$ L5 = 2000 nm, $N_d = 5.0\times10^{18}$ cm^{-3}
# 1567 Chalmers	InAs/AlSb/InAs Buffer: n+ InAs, and n+ GaAs Substrate: n+ GaAs Barrier thickness L3	L1 = 200 nm, $N_d = 5.0\times10^{18}$ cm^{-3} $L2_1$ = 320 nm, $N_d = 1.0\times10^{17}$ cm^{-3} $L2_2$ = 5 nm, undoped L3 = 25 nm, undoped $L4_2 = L2_2$, $L4_1 = L2_1$ L5 = 2000 nm, $N_d = 5.0\times10^{18}$ cm^{-3}
# ST1 Tampere	$In_{0.53}Ga_{0.47}As$/ $In_{0.52}Al_{0.48}As$/ $In_{0.53}Ga_{0.47}As$ Substrate: n+ InP Barrier thickness L3	L1 = 400 nm, $N_d = 4.0\times10^{18}$ cm^{-3} L2 = 400 nm, $N_d = 6.0\times10^{16}$ cm^{-3} L3 = 25 nm, $N_d = 6.0\times10^{16}$ cm^{-3} L4 = L2 L5 = 1000 nm, $N_d = 4.0\times10^{18}$ cm^{-3}
# 1047 IMEC	InAs/AlSb/InAs Buffer: n+ InAs, and n+ GaAs Substrate: n+ GaAs Barrier thickness L3	L1 = 200 nm, $N_d = 2.6\times10^{18}$ cm^{-3} L2 = 150 nm, $N_d = 1.0\times10^{17}$ cm^{-3} L3 = 14 nm, undoped L4 = L2 L5 =3000 nm, $N_d = 2.6\times10^{18}$ cm^{-3}

The effect of position dependent material parameters were implemented following the procedure of M. S. Lundstrom and R. J. Schuelke [11]. The program can readily be modified further for other heterostructure materials. Since the device is highly unipolar, we chose to only solve Poisson's equation and the electron current continuity equation. In our simulations for which $x < 0.45$, the conduction band-offset was set equal to 65% of the difference in the bandgap. A nonuniform grid-mesh is used to obtain the necessary accuracy and acceptable calculation times. The contact resistivity of the ohmic contact can be set to a value of choice. The thermionic emission current, which limits the current through the device, is calculated from the equation for a reverse biased Schottky diode, using a voltage dependent barrier-height obtained from the shape of the modelled conduction band. Even if field emission through the base of the barrier may be negligible, the thermionic field emission through the top of the biased barrier may be considerable [12], and it should not be neglected. Its effect on the current was modelled by using an effective barrier height, slightly lower than that obtained from the numerical simulation. A suitable value for the barrier lowering was determined from the modelled electric field in the barrier [9]. The diode differential capacitance, $C = dQ/dV \approx \Delta Q/\Delta V$ is determined numerically from the change ΔQ in the stored electric charge in the semiconductor for an incremental change ΔV in the applied voltage. The integration of charge is carried out to the middle of the barrier for single barrier devices. The details of the simulated device structures are summarized in Table II.

TABLE II
DETAILS OF MODELLED SBVS IN THE 3 × 60 GHz TRIPLER

Dev. ID	Layer thicknesses and doping concentrations			C_{max} [f F]	C_{min} [f F]	R_{slo} [Ω]
	Contact layer L1	Depl. layer: $L2_1 = L4_1$, $L2_2 = L4_2$	Barrier: $L3_1$, $L3_2$, $L3_3$			
# 100	L1 =100 nm, $N_d = 3.4\times10^{18}$ cm^{-3} $R_C = 2\times10^{-6}$ Ω cm^2	$L2_1$ =390 nm, $N_d = 1.0\times10^{17}$ cm^{-3}	L3 = 20 nm, $N_d = 1.0\times10^{15}$ cm^{-3}	23.4	3.1	33.0
# 101	Same as above	Same as above	L3 = 20 nm, $N_d = 1.0\times10^{16}$ cm^{-3}	23.7	3.1	33.0
# 102	Same as above	Same as above	L3 = 20 nm, $N_d = 1.0\times10^{17}$ cm^{-3}	26.4	3.2	33.0
# 103B	Same as above	Same as above	L3 = 20 nm, $N_d = 5.0\times10^{17}$ cm^{-3}	34.9	3.7	32.9
# 103	Same as above	Same as above	L3 = 20 nm, $N_d = 1.0\times10^{18}$ cm^{-3}	39.8	3.3	33.1
# 112	Same as above	$L2_1$ =386 nm, $N_d = 1.0\times10^{17}$ cm^{-3} to $N_d = 8.0\times10^{16}$ cm^{-3} $L2_2$ = 4 nm, $N_d = 5.0\times10^{17}$ cm^{-3}	$L3_1$ = 7 nm, $N_d = 1.0\times10^{18}$ cm^{-3} $L3_2$ = 6 nm, $N_d = 2.0\times10^{17}$ cm^{-3} $L3_3$ = 7 nm, $N_d = 1.0\times10^{18}$ cm^{-3}	39.1	3.7	34.1
# 114	Same as above	$L2_1$ =385 nm, $N_d = 2.0\times10^{17}$ cm^{-3} to $N_d = 1.0\times10^{15}$ cm^{-3} $L2_2$ = 5 nm, $N_d = 5.0\times10^{16}$ cm^{-3}	$L3_1$ = 6 nm, $N_d = 1.0\times10^{18}$ cm^{-3} $L3_2$ = 8 nm, $N_d = 5.0\times10^{16}$ cm^{-3} $L3_3$ = 6 nm, $N_d = 1.0\times10^{18}$ cm^{-3}	34.8	3.3	33.4

2.4 CV Characteristics and Conversion Efficiencies of Modelled Device Structures

It is of importance to understand how the CV characteristic can be modified by changes to the epitaxial structure. It is obvious that increasing the width of the barrier will decrease $C_{\max}$, and that wider $L2$ and $L4$ regions, see Fig. 1, will allow a larger capacitance swing, i.e., make $C_{\min}$ smaller. Below we will investigate how the doping profile of the diode affects the efficiency of a 3 × 60 GHz tripler. A modified version of the computer program by P. H. Siegel *et al.* [13] was used in the harmonic balance simulations. These simulations were made for GaAs/$Al_{0.44}Ga_{0.56}As$ rather than GaAs/$Al_{0.7}Ga_{0.3}As$ because of its smaller thermionic current.

The following rules are basic to the understanding of the behavior of the CV characteristic for different choices of doping concentrations, viz.

i. Doping the barrier will increase $C_{\max}$ without influencing the capacitance value at large bias voltages, i.e., $C_{\min}$ is not much affected. This phenomenon is studied in structures #100-103B, #103. However, too many dopants in the barrier will reduce the effective barrier height, and consequently the blocking capability of the barrier. The reduction in barrier height is caused by band bending adjacent to the barrier due to electron accumulation.

ii. A similar effect, an increase in $C_{\max}$, can be obtained by introducing thin regions with high doping concentration adjacent to the barrier on each side. One such example is structure #112. This scheme may be less damaging to the barrier's blocking capability, but it may also affect material quality in a negative way or make symmetrical growth more difficult.

iii. A reduced doping concentration in the $L2$ and $L4$ layers where the depletion occurs, will cause a more rapid change in the capacitance versus bias voltage. However, it will also lead to a larger series resistance. This method cannot therefore be recommended as a stand alone measure.

iv. To avoid an increase in the series resistance according to iii., a tapered doping concentration in the $L2$ and $L4$ region will improve the situation. A comparison between structures #112 and #114 illustrates this phenomenon, (see Fig. 8).

Note that the choice of doping profile will also influence the series resistance. The *total* series resistance has, in this paper, consistenly been calculated as the full Mesa resistance plus the contribution from the ohmic contact and the spreading resistance. Since part of the Mesa is always depleted, this approach will over estimate the series resistance.

The effect of doping the barrier on the CV characteristic is illustrated in Fig. 6 which shows the results for structures #100-103B, #103. The increase in $C_{\max}$ is as large as 70% when the doping is increased from $1 \times 10^{15}\,\mathrm{cm}^{-3}$ to $1 \times 10^{18}\,\mathrm{cm}^{-3}$. To see any effect at all, the doping in the barrier needs to exceed $1 \times 10^{17}\,\mathrm{cm}^{-3}$. The series resistance remains the same of course, since it is essentially determined by the doping in region $L2$ and $L4$ and the contact resistance. Fig. 7 shows the conversion efficiency versus input power (all input power is assumed to be absorbed). It is interesting to note that the efficiency actually decreases as $C_{\max}$ increases for a constant $C_{\min}$. This is in agreement with the results presented in Section 2.1.

Structures #112 and #114 both have linearly graded doping concentration in the $L2$ and $L4$ regions (see Table II). The effect of a high doping concentration adjacent to the barrier interface is illustrated by the CV characteristic of structure #112 in Fig. 8. Notice that the CV becomes almost identical to the one of structure #103. Since the series resistances are also very similar, the efficiencies versus pump power are virtually identical as can be seen from Fig. 7 and Fig. 9. When compared, the CV characteristics of structures #114 and #103B show roughly the same $C_{\max}$ and $C_{\min}$, for almost the same series resistance (Table II). It is therefore not surprising that the maximum efficiency of #112 is very similar to that of #103B. Hence, for these particular examples there is no improvement in the efficiency due to the linear

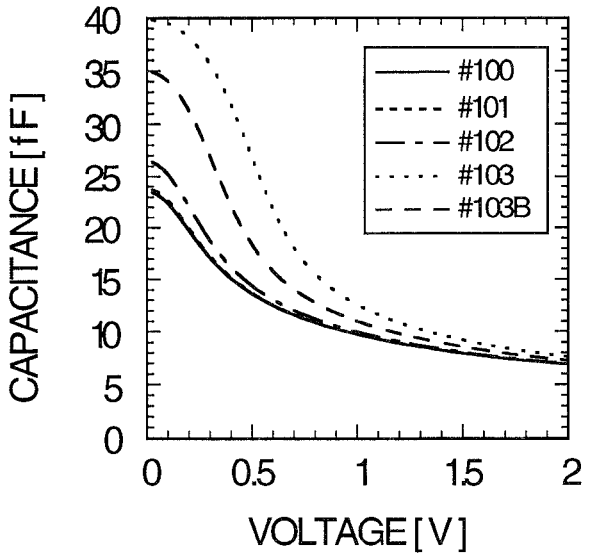

Fig. 6. Calculated CV characteristics for symmetric 10 μm^2 GaAs/$Al_{0.44}Ga_{0.56}As$ structures with different barrier doping concentrations: (ID #100) $N_d = 1.0 \times 10^{15}\,cm^{-3}$, (ID #101) $N_d = 1.0 \times 10^{16}\,cm^{-3}$, (ID #102) $N_d = 1.0 \times 10^{17}\,cm^{-3}$, (ID #103B) $N_d = 5.0 \times 10^{17}\,cm^{-3}$, (ID #103) $N_d = 1.0 \times 10^{18}\,cm^{-3}$. See Table II for further details.

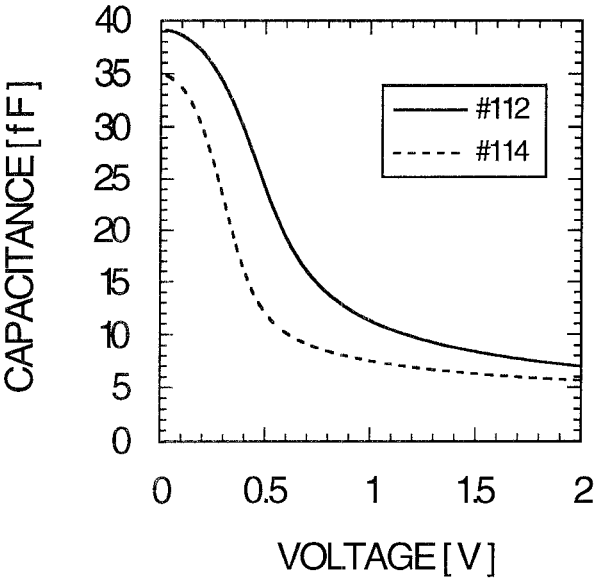

Fig. 8. Calculated CV characteristics for symmetric GaAs/$Al_{0.44}Ga_{0.56}As$ structures of size 10 μm^2 for different doping profiles in the $L2$ and $L4$ regions meant to enhance the C_{max}/C_{min} ratio. Structure \#112 has a small doping gradient, while structure #114 has a large doping gradient. See Table II for further details on the epitaxial layers.

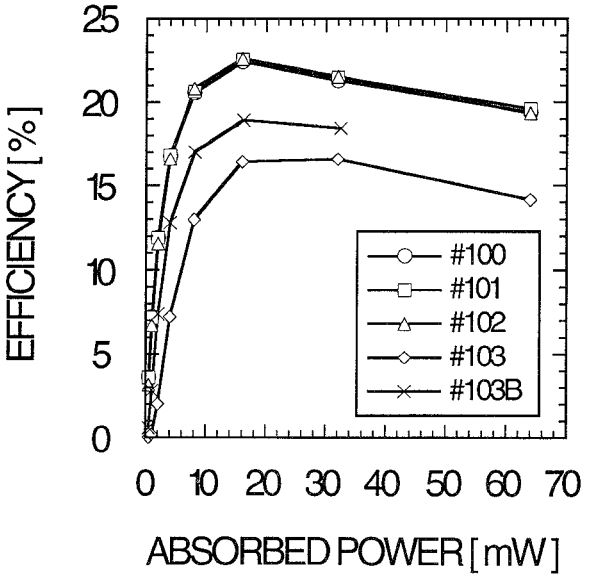

Fig. 7. Calculated conversion efficiency versus pump power for structures #100-103 and #103B at 3 × 60 GHz output frequency. Device area was 10 μm^2. Devices with an undoped or a low doped barrier have the highest conversion efficiency. The series resistance R_{slo} (at the pump frequency) was between 32.9 Ω and 33.1 Ω for all five structures, as calculated by the simulation program, and assuming an ohmic contact resistance of $2.0 \times 10^{-6}\,\Omega cm^2$.

doping gradient. However, a more systematic search for an optimally graded doping concentration, we believe, may be rewarding.

III. A 750 GHz Multiplier Design Study

A theoretical study of 750 GHz tripler multiplier configurations using GaAs and InAs SBV diodes is performed next. The desired output power from such a tripler is $\geq 50\,\mu W$ at 750 GHz, assumed to be enough for pumping a 750 GHz SIS mixer. The maximum available pump power from a solid state 250 GHz source (3 × 83 GHz tripler) for the 750 GHz tripler is assumed to be about 6 mW. This assumption is based on the fact that 11 mW of output power can be achieved from an optimized 250 GHz Schottky-varactor diode tripler, at operating conditions close to the Schottky diode burnout [16]. Since this might be a slightly optimistic number, and since one must also account for some losses in the SBV multiplier mount, it is reasonable to assume 6 mW as the available pump power at the SBV diode.

Different important diode parameters are investigated, such as the cutoff frequency which is a direct function of the doping concentration N_d in epilayers $L2$ and $L4$, in Fig. 1. The dynamic cutoff frequency is calculated for GaAs and InAs SBV diodes of two different sizes, see Fig. 10. The thickness of $L2$ and $L4$ are chosen so that these regions are completely depleted for a bias voltage equal to the breakdown voltage. It can be seen that the optimum doping concentration in $L2$ and $L4$ is $1 \times 10^{17}\,cm^{-3}$ for GaAs, and $2 \times 10^{17}\,cm^{-3}$ for InAs, both having a diameter of $2\,\mu m$.

Another parameter considered is the influence of plasma resonance on the series resistance of the diode [14]. This is of great importance to devices intended for THz frequencies. Fig. 11 shows the calculated series resistance for InAs SBV diodes when the plasma resonance effect is taken into account. It is found that by using InAs instead of GaAs, the plasma resonance frequencies are shifted to higher frequencies. This is due to the much higher electrical conductivity σ, of InAs compared to that of GaAs. It can also be seen in Fig. 11 that a doping N_d in $L2$ and $L4$ of about $1 \times 10^{17}\,cm^{-3}$ is acceptable up to 2 THz.

The avalanche breakdown voltage for epilayers $L2$ and $L4$ limits the maximum pump power that can be used for

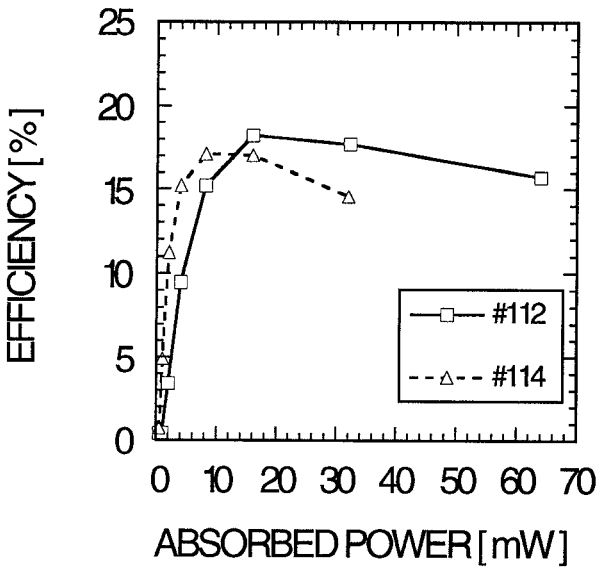

Fig. 9. Calculated conversion efficiency versus pump power for structures \#112 and \#114 of size 10 μm^2 at 3 x 60 GHz output frequency. See Table II for further details on the epitaxial layers.

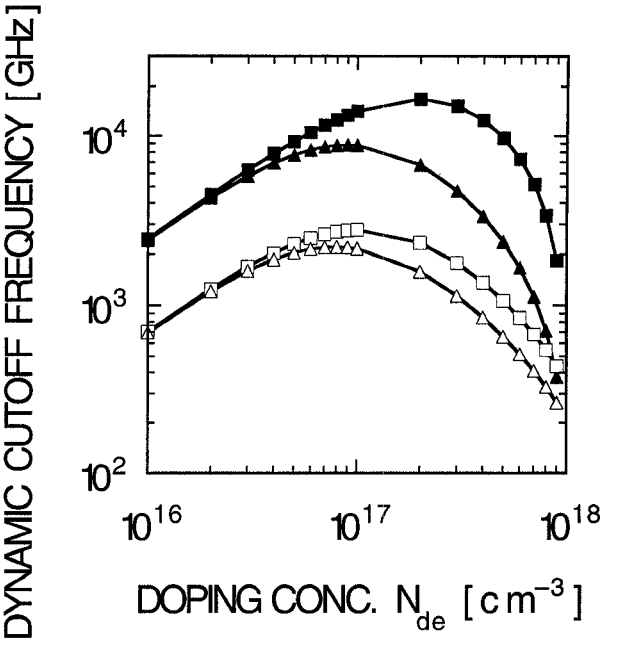

Fig. 10. Calculated dynamic cutoff frequency versus doping level N_{de} for GaAs and InAs SBV-diodes of two different diameters a. $N_{ds} = 3.4 \times 10^{18}\,cm^{-3}$ in $L1$ and $L5$, $N_{db} = 1 \times 10^{17}\,cm^{-3}$ in $L3$. $L1 = L5 = 100$ nm, $L2$ and $L4$ varies with N_{de}, the barrier width $L3$ is 20 nm. GaAs: (□): $a = 2\,\mu m$, (△): $a = 20\,\mu m$ InAs: (■): $a = 2\,\mu m$, (▲): $a = 20\,\mu m$

the device. Using the optimum doping concentration the breakdown voltage is calculated to be 15.7 V for GaAs and 1.2 V for InAs wth corresponding depletion lengths of 480 nm and 100 nm, respectively [15]. Due to the very small breakdown voltage for the doped InAs epilayers, the doping is reduced slightly to a constant value of $1 \times 10^{17}\,cm^{-3}$ which yields a breakdown voltage of 2 V and a depletion length of 179 nm.

The following structure in the InAs/AlSb/InAs material system is chosen for further study: Diode diameter 2 μm, $L1 =$ 100 nm with $N_d = 3.4 \times 10^{18}\,cm^{-3}$, $L2 = L4 = 150$ nm with $N_d = 1 \times 10^{17}\,cm^{-3}$, $L3 = 14$ nm with $N_d = 5 \times 10^{15}\,cm^{-3}$, and $L5 = L1 + 200$ nm. The total current through the SBV diode consists of (i) the conduction-current (mainly thermionic current), and (ii) the displacement current due to the RF voltage variation over the depletion region. In most cases we find that the conduction-current component has a negligible influence on the efficiency, see Fig. 12. In the calculations the *maximum* allowed input power is set to such a value that the RF voltage over the device, minus the RF voltage over the series resistance, is less than or equal to the breakdown voltage V_{br} of the doped epilayers $L2$ and $L4$. The plasma resonance effect on the series resistance is included in these calculations.

The calculated conversion efficiencies for 750 GHz SBV diode multipliers using SBV diodes based on InAs and GaAs are shown in Fig. 13. In order to evaluate what implications the choice of material has on the efficiency of a device (because of the much lower R_c possible with InAs), two different contact resistances, $R_c = 8 \times 10^{-7}\,\Omega cm^2$ and $1 \times 10^{-8}\,\Omega cm^2$, are used in simulations of GaAs SBV diodes. The higher electron mobility in InAs reduces the series resistance of the diode, thus giving InAs SBV diodes an advantage in efficiency over GaAs SBV diodes having the same ohmic contact resistance for low input powers. This advantage in efficiency is more evident when a more realistic ohmic contact resistance of $8 \times 10^{-7}\,\Omega cm^2$ is used for the GaAs SBV diodes.

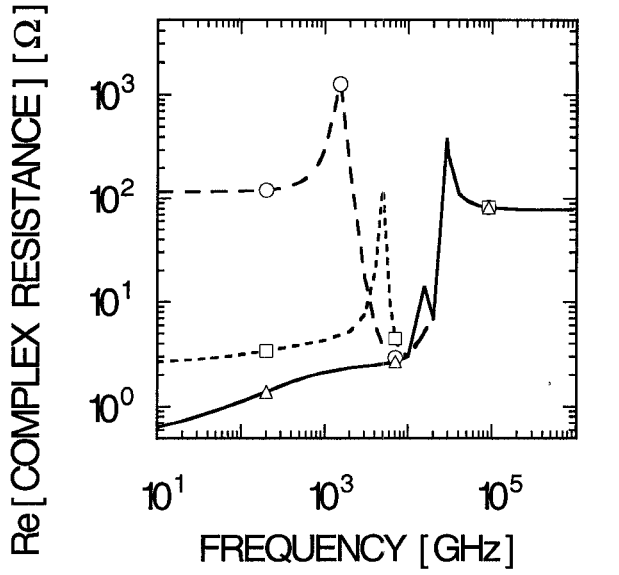

Fig. 11. Real part of calculated complex resistance versus pump frequency for an InAs SBV diode for different doping levels N_{de} in the low doped epilayers $L2$ and $L4$. Doping concentration $N_{ds} = 3.4 \times 10^{18}\,cm^{-3}$ in $L1$ and $L5$, $N_b = 1 \times 10^{17}\,cm^{-3}$ in the barrier $L3$, $L1 = L5 = 100$ nm, $L2 = L4 = 533$ nm, $L3 = 20$ nm, diameter $a = 3.57\,\mu m$. (○): N_{de} is $1 \times 10^{16}\,cm^{-3}$ (□): N_{de} is $1 \times 10^{17}\,cm^{-3}$ (△): N_{de} is $1 \times 10^{18}\,cm^{-3}$

Using a larger diameter SBV diode means of course a lower impedance, while it can handle a larger input power before V_{RF} exceeds the breakdown voltage V_{br}. A larger diameter device will also withstand larger absorbed pump power, before efficiency degradation occurs due to the reduced mobility, μ, of the electrons, caused by increased thermal heating.

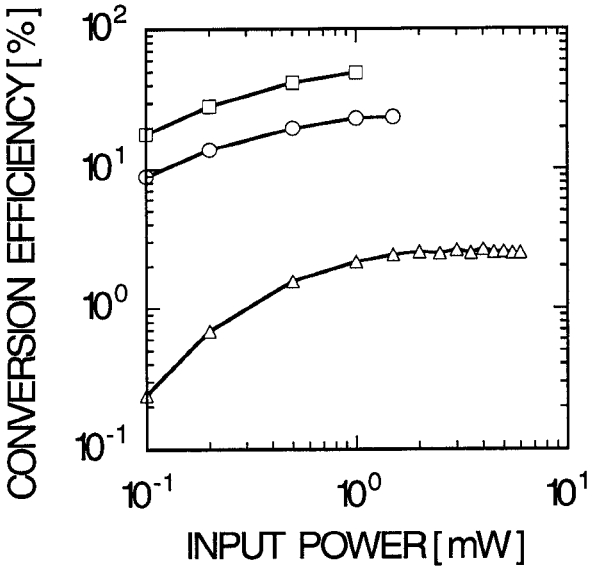

Fig. 12. Calculated conversion efficiency versus input power, when varying the calculated conductance, dI/dV, for the device in steps of $(dI/dV)\times 10^y$, where y is 0, 2, or 3. The assumed SBV diode structure is described in the text. For the case $y = 0$ the theoretical IV characteristic was used. The diode diameter, $a = 2\,\mu$m. (□): $y = 0.0$, (o): $= 2.0$, (△): $y = 3.0$

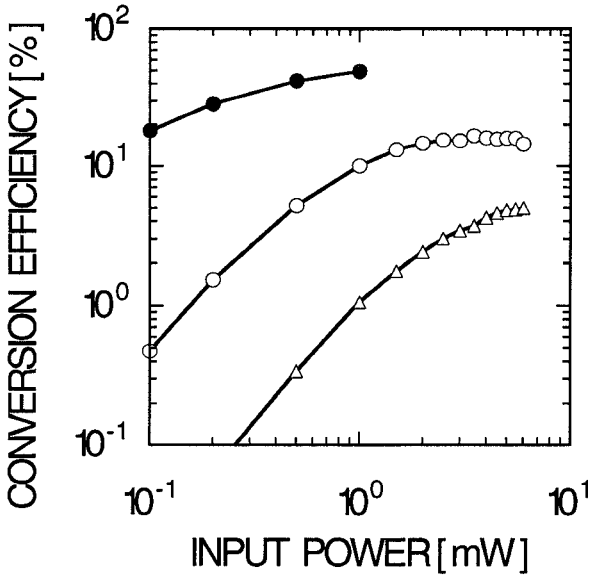

Fig. 13. Calculated conversion efficiency versus power for a 750 GHz tripler configuration using InAs and GaAs SBV diodes as the nonlinear element. $R_{co} = 1 \times 10^{-8}\,\Omega\text{cm}^2$. The assumed SBV-diode structure used in the calculations is equal to the chosen structure, see text. The diode diameter $a = 2\,\mu$m. (o): GaAs SBV diode tripler, $R_c = R_{co}$ (△): GaAs SBV diode tripler, $R_c = 80 \times R_{co}$ (•): InAs SBV diode tripler, $R_c = R_{co}$

Approximately for GaAs, $\mu \sim T^{-1}$ and for InAs: $\mu \sim T^{-3/2}$ [17]–[19]. InAs is obviously more sensitive to heating than GaAs. However, in this investigation we find that in neither of the material systems is thermal heating likely to become a problem. Since the level of absorbed pump power is already restricted by the pump source itself, the low breakdown voltage of InAs is acceptable.

The calculated output power, using the values for the efficiency shown in Fig. 13, is shown in Fig. 14. The simulated

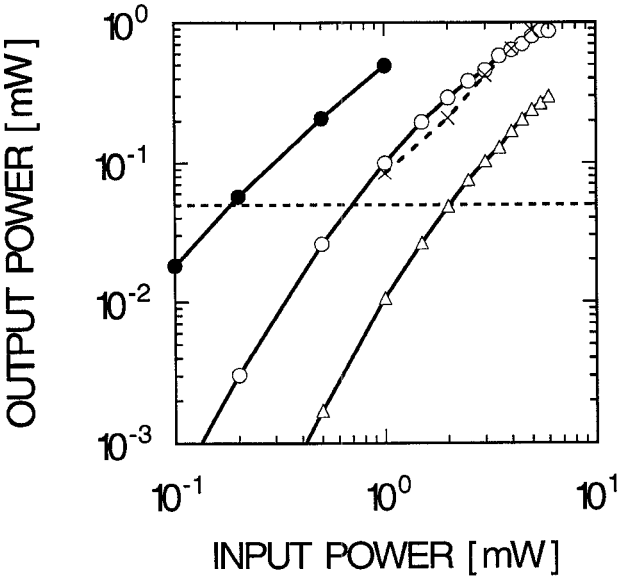

Fig. 14. Calculated output power versus input power for a 750 GHz tripler configuration, using InAs and GaAs SBV diodes and a Schottky-varactor diode as the nonlinear element in the multiplier. See Fig. 13 for further information. (×): Schottky-varactor tripler with $C_0 = 2.8$ fF and $R_s = 20\,\Omega$ [20].

output power for a state of the art 2.8 fF Schottky-varactor diode described in [20], is also shown in Fig. 14. It can be seen that the theoretical maximum output power for the Schottky-varactor diode clearly exceeds the output power of the GaAs SBV diode multipliers having a realistic ohmic contact resistance, R_c of $8 \times 10^{-7}\,\Omega\text{cm}^2$. However, the InAs SBV has a much higher efficiency than the Schottky multiplier at low pump powers.

It should be noted that the calculation for the Schottky-varactor tripler assumes optimum embedding impedance at all frequencies, i.e., including the idler. For the SBV diode tripler, optimum embedding is only required for the input and output frequencies. Thus the optimum conditions are much easier to obtain for the SBV diode than for the Schottky-varactor diode, in reality giving the SBV diode an advantage in efficiency compared to the Schottky-varactor diode. Also the unavoidable resistive losses at the idler frequency in the Schottky-varactor diode tripler gives the SBV diode tripler another advantage. The expected loss in the 750 GHz tripler mount is less than 10 dB [20]. However, it can be seen from Fig. 14 that the only realistic SBV diode capable of generating $\geq 500\,\mu$W, necessary for $\geq 50\,\mu$W of output power at 750 GHz is the InAs based diode. This performance is achieved close to the point when the maximum RF voltage becomes equal to the breakdown voltage. This disadvantage can perhaps be compensated for by connecting several InAs/AlSb junctions in series, creating a multiple barrier InAs SBV diode (see Section 2.1).

Also note that the GaAs SBV diode with $R_c = 8 \times 10^{-7}\,\Omega\text{cm}^2$, could in principle be pumped by a much larger input power than 6 mW, used in Fig. 14 as a maximum, before the diode voltage exceeds the breakdown voltage of the device. The dotted line in Fig. 14 marks the minimum 50 μW output power which we use as a design goal, assuming no losses in the mount. The efficiency for the InAs SBV at 500 μW output

is 50%. It can easily be shown that this number agrees well with the study presented in Section 2.1. The InAs varactor has a dynamic cutoff frequency of 14 THz according to Fig. 10, yielding $1/(2\pi R_s C_{\min}) \approx 20$ THz. With a pump frequency of 250 GHz and the normalized $1/(\omega_p C_{\min}) = 100\,\Omega$, we have $R_s = 100 \times (250/20000) = 1.25\,\Omega$, suggesting a maximum efficiency of the order 50%. This nice agreement certainly encourages use of the *rules of thumb,* derived in Section 2.1, for device optimization.

IV. Conclusions

Theoretical work on triplers employing SBV diodes show a maximum efficiency for a lower $C_{\max}$ to $C_{\min}$ ratio than initially expected. An efficiency maximum exists for $C_{\max}/C_{\min} \approx 2.5$. This has been shown both in simplified calculations using a sinusoidal CV characteristic as well as in full harmonic balance simulations using realistic CV characteristics. These findings have important implications. There is no need for a thin barrier, instead a thicker barrier can provide an extra reduction in current. A low contact resistance is very important in order to obtain a high conversion efficiency. For material systems which are lattice mismatched, such as the InAs/AlSb system, there is an upper limit on the total barrier thickness. The examples presented can be used as *design guidelines.* In a case study for a 750 GHz multiplier an InAs SBV diode clearly outperforms a Schottky diode. SBV diodes can also be used in very high efficiency multipliers in the microwave frequency range.

Acknowledgment

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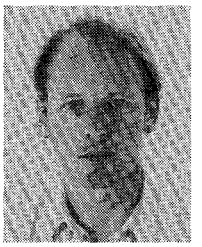
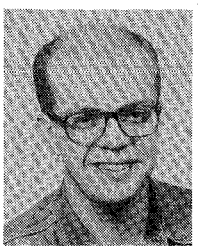
Svein M. Nilsen was born in Drammen, Norway in 1956. He received the MSEE and Technical Licentiate degrees from Chalmers University of Technology, Sweden in 1980 and 1986, respectively. He is currently working towards his Ph.D.

Since 1982 he has worked on GaAs devices for mm-wave applications, and device fabrication technologies at Chalmers University of Technology. From 1986 to 1989 he worked part time as Process Manager at The Microelectronics Applied Research Institute (MARI) in Göteborg, Sweden.



Hans Grönqvist was born in Pernå, Finland, in 1958. He received the Masters degree in 1987, and the degree of Licentiate of Engineering in 1990, both from Chalmers University of Technology, Göteborg, Sweden. He is currently working towards his Ph.D.

Mr. Grönqvist's interests are heterostructure devices such as the Single Barrier Diode and the Heterostructure Field Effect Transistor.



Hans Hjelmgren received the M.Sc. and Ph.D. degrees from Chalmers University of Technology, Sweden, in 1984 and 1991, respectively.

He has been working with numerical modelling of Schottky diodes and heterojunction structures since 1987. As a part of his Ph.D. studies, he spent eight months during 1990 at the University of Leeds, England. Since the beginning of 1992 he has been working as a Visiting Postdoctoral Research Associate at the University of Massachusetts, Amherst.

Anders Rydberg was born in Lund, Sweden, in 1952. He received the M.Sc. degree from Lund Institute of Technology in 1976. He worked for two years with microwave technology at the National Defense Research Establishment in Linköping, after which he joined the ELLEMTEL Development Company for one year. In 1986 and 1988 he received the degree of Licentiate of Engineering and the Ph.D. degree respectively from Chalmers University of Technology. Between 1990 and 1991 he worked as a senior research engineer at Farran Technology Ltd. in Ireland. In 1991 he was appointed Docent in Applied Electron Physics at Chalmers University of Technology. In 1992 he became Associated Professor at the Circuits and Systems Group at Uppsala University School of Technology.

His main interests are micro-, and millimeter-wave solid state components and circuits for power generation. He has published more than 40 papers in the above research area and was co-author of a chapter in *Coherent Detection at Millimeter Wavelengths and Their Applications,* Nova Science Publishers Inc., New York 1991.

Erik L. Kollberg (M'83–SM'83–F'91) received the M.Sc. degree in 1961 and the Teknologie Doktor degree in 1971 from Chalmers University of Technology, Gothenburg, Sweden.

He has been a Professor at Chalmers University of Technology since 1974. Most of his work has been focused on low noise receiver technology for applications in radio astronomy at Onsala Space Observatory, and he has published more than 150 papers. From 1963 to 1976 he performed research on low-noise maser amplifiers. Various types of masers were developed for the frequency range 1 GHz to 35 GHz. In 1972 research was initiated on low-noise millimeter wave Schottky diode mixers, and 1981 also on millimeter and submillimeter wave superconducting quasiparticle mixers. Recently he has broadened his interest in high Tc superconducting circuits and semiconductor devices, including various kinds of diodes and three terminal devices. He was on six months sabbatical leave at the California Institute of Technology, Pasadena, unitl March 1991.

Dr. Kollberg was the winner of the 1982 Microwave Prize given at the 12th European Microwave Conference in Helsinki, Finland and was awarded the Gustaf Dahlén gold medal 1986.